Amendments to the Claims

The following Listing of Claims replaces all prior listings, and versions, of claims in the present application.

Listing of Claims:

1. (Currently Amended) A method of identifying a plurality of transponders in an interrogation process comprising:

transmitting an interrogation signal to the transponders;

receiving a response signal from each transponder at a time within a respective waiting period the maximum duration of which can be adjusted;

creating a plurality of data line signals together defining a random number;

feeding said data line signals to a counter on respective ones of a plurality of data lines for determining the waiting period; and

providing at least one of the data lines with logic circuitry ~~whereby~~ wherein ~~control of~~ the logic circuitry is configured to control the at least one of the data lines to ~~can~~ block or permit the respective data line signal to be received by the counter thereby adjusting ~~thea~~ total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

2. (Currently Amended) A method of identifying a plurality of transponders in an interrogation process comprising:

transmitting an interrogation signal to the transponders;

receiving a response signal from each transponder during a respective waiting period, ~~thea~~ maximum duration of ~~which~~the waiting period being adjustable ~~can be adjusted, the transponder having a random number generator and a counter~~; and

for each transponder:

transmitting output signals on respective ones of a plurality of data lines from ~~the~~ a random number generator of the transponder to respective inputs of ~~the~~a counter of the transponder for determining the waiting period, at least one of the output signals from the random number generator being fed via logic circuitry to a respective input of the counter~~:~~; and

controlling the logic circuitry to adjust the maximum length of the waiting period.

3. (Previously presented) A method as claimed in claim 1, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines.

4. (Previously presented) A method as claimed in claim 1, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

5. (Original) A method as claimed in claim 4, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

6. (Previously presented) A method as claimed in claim 1, wherein by controlling the logic circuitry the maximum duration of the waiting period is increased or decreased by multiples of 2 or 0.5 respectively.

7. (Currently Amended) A method as claimed in claim 5, wherein by controlling the logic circuitry the desired Round Size is selected by increasing or decreasing the number of minimum Round Sizes to be combined, wherein ~~the~~ available different Round Sizes ~~available being~~ are related to one another by factors or multiples of 2 or 0.5.

8. (Previously presented) A method as claimed in claim 2, including the step of clocking the random number generator and/or clocking the counter by means of a clock oscillator of the transponder.

9. (Original) A method as claimed in claim 8, including causing the transponder to transmit an output signal from its transmitter when the counter has been counted to its terminal count, whereupon the counter loads a fresh or new number from the random number generator for the next count.

10. (Currently Amended) A method as claimed in claim 8, comprising determining the maximum possible waiting time or maximum possible number of slots over which to randomize transmissions of the output signal from the transmitter by the length of the counter, the data lines between the random number generator and the counter being gated in order to "fold" the counter such that the effective counter length may be modified in multiples of two.

11. (Previously presented) A method as claimed in claim 1, including deriving the random number by taking a snapshot of the transponder clock, or by a hash value received from the interrogator in a command.

12. (Previously presented) A method as claimed in claim 1, including using either an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

13. (Previously presented) A method as claimed in claim 1, wherein the output response signal contains identity or field data of a tag or transponder.

14. (Previously presented) A method as claimed in any claim 1, wherein transponders not already included in an active population under interrogation are arranged to enter said active

population, whereupon said transponders entering the active population receive a signal from the interrogator to adjust the maximum length of their waiting period.

15. (Original) A method as claimed in claim 14, wherein the adjusted maximum length of the waiting period of the transponders, after arriving into an already existing active population under interrogation, is chosen to ensure transmissions from said transponders occur at an appropriate stage in the arbitration to facilitate reading of those transponders entering the active population.

16. (Previously presented) A method as claimed in claim 14, wherein the transponders are moving relative to the interrogator.

17. (Currently Amended) A transponder ~~for generating an output signal during a waiting period,~~ comprising:

means for deriving a random number within the transponder; and

means for delivering the random number by way of binary output signals along respective ones of a plurality of data lines to a counter, wherein at least one of the data lines is connected to the counter via logic circuitry, wherein control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

18. (Currently Amended) A transponder ~~for generating an output signal during a waiting period, the transponder~~ comprising:

a random number generator configured to generate ~~the~~ binary output signals on respective ones of a plurality of data lines ~~from~~ which are fed to the inputs of a counter for determining the waiting period, wherein at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period. 19. (Currently Amended) A transponder as

claimed in claim ~~14~~17, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines for the binary output signals.

20. (Currently Amended) A transponder as claimed in claim ~~14~~17, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

21. (Original) A transponder as claimed in claim 17, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

22. (Currently Amended) A transponder as claimed in claim ~~14~~17, wherein the logic circuitry is arranged to enable the maximum duration of the waiting period to be increased or decreased by multiples of 2 or 0.5 respectively.

23. (Currently Amended) A transponder as claimed in claim 18, wherein the logic circuitry is arranged to enable the desired Round Size to be selected by increasing or decreasing the number of minimum Round Sizes to be combined, wherein ~~the~~ available different Round Sizes ~~available being~~are related to one another by factors or multiples of 2 or 0.5.

24. (Currently Amended) A transponder as claimed in any claim ~~14~~17, wherein the transponder dynamically alters the maximum waiting time in response to an instruction from an interrogator.

25. (Currently Amended) A transponder as claimed in claim ~~14~~17, wherein the transponder is adapted to detect either heavy signal congestion or large quiet signal periods and alter the maximum waiting time accordingly.

26. (Currently Amended) A transponder as claimed in claim ~~14~~17, wherein the transponder is adapted to alter the maximum waiting time in response to an instruction from the interrogator or in response to external conditions present during the interrogation.

27. (Currently Amended) A transponder comprising:

a receiver for receiving an interrogation signal from an interrogator;

a transmitter for transmitting a response signal after receipt of the interrogation signal;

means for generating the response signal during a waiting period; and

a random number generator for generating ~~the~~ binary output signals ~~from~~ which are fed via respective ones of a plurality of data lines to ~~the~~ inputs of a counter for determining the waiting period, wherein at least one of the output signals from the random number generator is fed via a data line having logic circuitry to a respective input of the counter, wherein control of the logic circuitry adjusts the maximum length of the waiting period during interrogation by the interrogator.

28. (Canceled)

29. (Currently Amended) A transponder as claimed in claim ~~14~~17, wherein the random number is derived by taking a snapshot of the transponder clock, or by a hash value received from a command from an interrogator.

30. (Currently Amended) A transponder as claimed in claim ~~14~~17, wherein the counter is an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

31. (Currently Amended) A transponder as claimed in claim ~~14~~17, including a memory for storing an identity or data field and a modulator for transmitting the identity or data as a message in the output response signal.

32. (Currently Amended) An identification system comprising:

an interrogator, and

a plurality of transponders,

the interrogator including a transmitter for transmitting an interrogation signal to the transponders,

each transponder including:

a receiver for receiving the interrogation signal,

a transmitter for transmitting a response signal after receipt of the interrogation signal, and

means for generating the response signal during a waiting period,

each transponder having means for altering ~~the~~ a maximum length of the waiting period during interrogation of the transponders by the interrogator,

the transponder further including a random number generator for generating ~~the~~ binary output signals ~~from~~ which are fed via respective ones of a plurality of data lines to the inputs of a counter for determining the waiting period,

wherein at least one of the output signals from the random number generator is fed via a data line having logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period.

33. (Currently Amended) An identification system comprising:

an interrogator, and

a plurality of transponders,

the interrogator including a transmitter for transmitting an interrogation signal to the transponders,

each transponder including:

a receiver for receiving the interrogation signal,

a transmitter for transmitting a response signal after receipt of the interrogation signal, ~~and~~

means for generating the response signal during a waiting period, ~~each transponder having~~

means for altering the maximum length of the waiting period during interrogation of the transponders by the interrogator, ~~the transponders having~~

means for deriving a random number within the transponder and delivering the random number by way of binary output signals along respective ones of a plurality of data lines to a counter,

wherein at least one of the data lines is connected to the counter via logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

34. (Canceled)

35. (Currently Amended) An integrated circuit for use in a transponder of an RFID interrogation system, the integrated circuit comprising:

a receiver for receiving an interrogation signal;

a transmitter for transmitting a response signal after receipt of the interrogation signal;

means for generating the response signal during a waiting period; ~~and~~

control means for altering the maximum length of the waiting period;

means for deriving a random number within the integrated circuit and delivering the random number by way of binary output signals along respective ones of a plurality of data lines to a counter and wherein at least one of the data lines is connected to the counter via logic circuitry control of which can block or permit the data line signal to the counter thereby adjusting ~~the~~a total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

36. (Currently Amended) An integrated circuit for use in a transponder comprising:

a receiver for receiving an interrogation signal;

a transmitter for transmitting a response signal after receipt of the interrogation signal;

means for generating the response signal during a waiting period;

control means for altering the maximum length of the waiting period during interrogation of the transponder by the interrogator~~;~~:

a random number generator for generating ~~the~~ binary output signals ~~from~~ which are fed via respective ones of a plurality of data lines to the inputs of a counter for determining the waiting period;

a logic circuitry, wherein at least one of the output signals from the random number generator is fed via the logic circuitry to a respective input of the counter, control of the logic circuitry thereby providing means for adjusting the maximum length of the waiting period.

37. (Previously presented) An integrated circuit as claimed in claim 32, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines for the binary output signals to the counter.

38. (Previously presented) An integrated circuit as claimed in claim 32, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

39. (Original) An integrated circuit as claimed in claim 35, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

40. (Previously presented) An integrated circuit as claimed in claim 32, wherein the logic circuitry is arranged to enable the maximum duration of the waiting period to be increased or decreased by multiples of 2 or 0.5 respectively.

41. (Currently Amended) An integrated circuit as claimed in claim 36, wherein the logic circuitry is arranged to enable the desired Round Size to be selected by increasing or decreasing the number of minimum Round Sizes to be combined, wherein ~~the~~ available different Round Sizes ~~available being~~are related to one another by factors or multiples of 2 or 0.5.

42. (Currently Amended) An integrated circuit as claimed in claim 32, wherein the random number is derived by taking a snapshot of the transponder clock, or by a hash value received from a command from an interrogator.

43. (Previously presented) An integrated circuit as claimed in claim 32, wherein the counter is an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

44. (Previously presented) An integrated circuit as claimed in claim 32, including a memory for storing an identity or data field and a modulator for transmitting the data in the output response signal.

45. (Currently Amended) A reader for identifying a plurality of transponders, the reader comprising:

a transmitter for transmitting a reader signal to the transponders;

a receiver for receiving response signals from each transponder at a time within a respective waiting period the maximum duration of which can be adjusted; and

a processor for identifying a transponder from data in the response signal,

wherein the reader comprises detection means for detecting the number of collisions between response signals received at the receiver and control means for controlling the reader signal to control logic circuitry configured to control at least one of a plurality of binary output signals that are fed via respective ones of a plurality of data lines connected to a counter in the transponder to adjust the maximum length of the waiting period.

46. (New) The method of claim 1, wherein providing the at least one logic circuitry includes providing the at least one logic circuitry to control the at least one of the data lines, but not all of the data lines.